A 25-Gb/s × 4-Ch, 8 × 8 mm², 2.8-mm Thick Compact Optical Transceiver Module for On-Board Optical Interconnect

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Abstract: A 25-Gb/s × 4-ch optical transceiver module was developed. To obtain a compact module, CMOS analog front-end ICs, a lens integrated connector, and small LGA package was applied. The module demonstrated 25-Gb/s error-free transmission.

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1. Introduction

The bandwidths of information and communication technologies (ICT) systems such as servers and routers continue to grow, driven by the continually increasing use of the Internet and the growing demand for high-definition images and video data. In recent years, bandwidth has doubled every two years. It is predicted to reach about 10-Tb/s in 2015, while the backplane data rate is predicted to be 25-Gb/s in the same year. However, electrical transmission becomes increasingly problematic at high data rates due to higher loss and crosstalk. Thus, on-board optical modules for board to board interconnection have been discussed a lot for data rates exceeding 25-Gb/s [1-3].

A board to board interconnection has to have higher density compared with a rack to rack interconnection, which is used for active optical cables. Hence, an on-board optical module is required to be compact, have a low profile, and be low power for being arranged near the CPU or switch (SW) LSI.

In this paper, we propose a compact optical transceiver module with CMOS analog front-end ICs, a lens integrated connector, and small LGA package. The CMOS analog front-end IC realizes low power and high speed. The lens integrated connector realizes a low profile and high efficient heat radiation. The LGA package, which has different levels enables a miniature size and easy assembly by wire bonding. The fabricated 4-ch module successfully demonstrated 25-Gb/s operation. The module is a size of 8 × 8 mm², a t = 2.8-mm–thin, which is most compact in previously reported multi-channel transceivers exceeding 25-Gb/s.

2. Compact optical transceiver module design

The structure of the proposed optical transceiver module is shown in Fig. 1. The module is a pigtail one with 50-μm MMFs. A 850-nm 4-ch VCSEL array and a PD array are mounted face up and wire-bonded to the signal line on the package. A 4-ch VCSEL driver and a TIA are mounted on the package by flip chip bonding. A connector has a 45-degree mirror and 12-ch undersurface lenses. The package uses a low temperature co-fired ceramics (LTCC) to obtain flat surface, fine pattern and low resistance.

A. CMOS analog front-end IC

Block diagrams of the CMOS analog front-end ICs are shown in Fig. 2.

The VCSEL driver consists of a receiver, a pre-driver, a main driver, and an asymmetric emphasis circuit. The receiver has an equalizer for compensating for the loss of the line between LSIs, such as a CPU or SW, and the module. The pre-driver uses inductor peaking to achieve 25 Gb/s. The asymmetric emphasis circuit generates emphasis pulses by using a delay circuit. Furthermore, it is able to make the emphasis pulses be asymmetric between the rise time and fall time to suppress the nonlinear response of the VCSEL.

The TIA consists of a pre-amplifier, a post-amplifier, and output driver. To achieve a bandwidth of 25 Gb/s, a regulated-cascode (RGC) is applied as a pre-amplifier. Furthermore, to alleviate degradation of optical link due to power supply noise, we introduce a noise canceller and on-chip regulator [4]. The output driver is able to control peaking up to 7.7 dB to compensate for the line loss between the module and the LSI.
The VCSEL driver and the TIA were fabricated by using standard 65-nm CMOS technology. They consume 1.17 W, 11.7 mW/Gb/s/ch in total.

B. Lens integrated connector

The appearance of the lens integrated connector is shown in Fig. 3. The light beam from the VCSEL propagates upwards, is concentrated by the aspherical lens on the undersurface of the connector, and is coupled to 50-μm MMFs after being reflected by a 45-degree mirror. The mirror and lenses are formed at 0.5 mm from the connector edge. To put the mirror and lenses near the connector edge, a larger heat spreader is acquired, and it is able to improve the efficiency of heat radiation as well as enable a more compact package. Furthermore, we applied a one-lens optical interface structure, and the optical module achieves a low profile. Fibers are aligned by a V-groove formed on the connector. The connector size is 4 × 4.8 mm with a thickness of 1.7 mm. The coupling loss of the connector achieved a total of -2.7 dB in the Tx and Rx (Fig. 4).

C. Small LGA package

The LGA package has three different surface levels. One is the level of the VCSEL driver and TIA chip mounting. The chips are mounted on the package by flip-chip bonding. The output pads of the VCSEL driver and the input pads of the TIA are placed on a grounded coplanar line. The VCSEL and PD are wire-bonded on the other side of the line. The VCSEL and PD are mounted on the level that is 150 μm lower than the chip mounting level. To make 25-Gb/s operation possible, the VCSEL/PD’s surface is coordinated to the first level of package so that it is possible to minimize the length of the wire. The third level is placed on both sides of the package near the optical device, which is 200 μm higher than the first level. The lens integrated connector is put down on the third level, so the distance between VCSEL/PD’s surface and lens is decided by the third level height.

The output line of the VCSEL driver and the input line of the TIA are designed as grounded coplanar lines, and VDD lines for the PD’s cathode and ground lines, which are drawn on both sides of the signal line, are connected to the lower solid pattern layer to reduce line impedance. A 1-mm-wide ground plane is placed between the VCSEL driver and TIA. As a result, crosstalk between channels is able to be reduced below -36 dB, and crosstalk between the Tx and Rx is able to be reduced below -70 dB.
The transceiver module uses a 1.0-V and 3.3-V power supply. To minimize the package size, it is necessary to optimize the on-chip capacitor and on-package capacitor by designing power integrity. We used PEEC model to chip’s power line and executed chip-package co-design. The chip-package antiresonance are cancelled by mounting three different capacitors on package.

3. Experimental results

A compact optical transceiver module was fabricated by mounting an 850-nm VCSEL array, PD array, VCSEL driver chip, TIA chip, and lens integrated connector on an 11-layer LTCC package. A photograph is shown in Fig. 5. The module size was $8 \times 8 \text{ mm}^2$ with a thickness of 2.8 mm. The optical transceiver module demonstrated 25-Gb/s transmission, so the density of the module reached 1.56-Gb/s/mm$^2$.

The measured optical eye pattern of the Tx output is shown in Fig. 6(a), and the electrical eye pattern of the Rx output is shown in Fig. 6(b). A clear-opening was obtained for both the Tx output and Rx output after transmission in 1.5-m graded-index (GI) 50-μm MMFs. Furthermore, the module demonstrated 25-Gb/s error-free operation in each channel at a BER of $1 \times 10^{-12}$ with a PRBS pattern of $2^{29}-1$. The module consumed 11.7-mW/Gb/s/ch, 1.17-W in total.

4. Summary

We developed a compact optical module. To introduce low power CMOS analog front-end ICs, a low profile lens integrated connector and small LGA package with three different surface levels enables a compact size of $8 \times 8 \text{ mm}^2$, a t = 2.8-mm-thin module, 1.17-W low power consumption, and 25-Gb/s operation. This proposed module is suitable for next generation ICT systems.

5. References